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| **Dineshkumar Bhaskaran**  ☎: - (778) 893 8274 **✉**: - [dineshkumarb@gmail.com](mailto:dineshkumarb@gmail.com) | | | |
| **Summary** | | | |
| * Expert in high-performance parallel computing with a focus on algorithm parallelization, optimization, and benchmarking in areas like AI/ML, image processing, and distributed storage. * Extensive background in storage virtualization, Linux kernel development and board bring-ups. | | | |
| **Employment** | |  |  |
| **Senior member of technical staff** | | **AMD India** | Aug 2019 - till date |
| Rapids – Accelerated Data Science for ROCm:   * Ongoing activity for adopting Rapids projects for implementing popular pyData libraries for data science application on AMD GPU for ROCm stack. Owner for rapids’ CUDF projects like rapids-cmake, rapids memory manager (RMM), and NVComp. CUDF is a close substitution for pandas.   MLPerf Inferencing   * Implemented python reference code for models resnet50, yolov4 and Bert on AMD Instinct GPUs for multiple backends like pytorch, tensorflow, Tensor virtual machine (TVM) and MIGraphX. Implemented C++ lightweight inference server for resnet50 on TVM and improved performances by 51.5%.   ROCm Clang compiler   * [ROCm Compiler Support](https://github.com/RadeonOpenCompute/ROCm-CompilerSupport) maintainer from Aug 2019 to Sept. 2021. * Implementation of Multithreading and in-memory compilation support for AMDs lightning compiler (based on LLVM). In-memory compilation improved overall compilation process by 1.07% on Linux and ~29% on windows. | | | |
| **Principal Engineer** | | Capgemini Engineering (previously Aricent) | Oct 2017 – Jul 2019 |
| * Led efforts to create an accelerated storage I/O library using GPUs. Developed parallel and improved erasure-code algorithms in CEPH. This work was presented at SNIA SDC India and then Santa Clara under the title [“Accelerated Erasure Coding: The New Frontiers of Software-Defined Storage – 2018”](https://www.snia.org/events/storage-developer/presentations18). * Led a team to create software defined radio solution for Aricent. Involved in offloading FFT algorithm in OpenAirInterface 4G stack with NVIDIA GPUs and Xilinx FPGAs. | | | |
| **Principal Engineer** | | **Canon Inc** | **Mar 2010 - Oct 2017** |
| * Led a team to create an efficient medical image processing library for Canon medical apparatuses. Parallelized and optimized Image registration algorithm components like Pre-processing algorithms, Optimizers (Powell, LM, GD, SGD), Metrics (MI, NMI, RIU, SSD), transformation algorithms, and Resampler. * Managed and lead a team, that maintained and enhanced Linux based OS for Canon embedded products. Involved in porting Linux kernel and essential system applications to various ARM based SoCs. | | | |
| **Software Engineer** | Early Experience (Brocade Communications, Tata Elxsi) | | Sep 2003 - Mar 2010 |
| * Worked on Brocade Storage Application Services. SAS service include storage virtualization, online data migration, CDR, and CDP. Owner for virtualized initiator module in SAS solution. * Worked on Target Mode driver for LSI logic FC HBAs based on LSI-Logic Fusion message passing technology to act as a virtualized storage box. | | | |
| **Education** | | | |
| * Deep Learning Theory and Practice, IISc Bangalore, India * M.S Software systems 2006-2009, BITS Pilani, India * Bachelor of Technology, Computer Engineering 1999-2003, University of Calicut, Kerala, India. | | | |
| **Languages and Technologies** | | | |
| *Programming Languages:* C, HIP, OpenCL, familiar with CUDA, C++, Python, PTX, HLSL, ARM, X86 assembly.  *Protocols stacks:* FC, Familiar with SCSI, USB, OpenAirInterface 4G stack in Linux Kernel.  *Tools and ASICs:* ROCm and GNU Toolchain, Xilinx ZC-702/706, TI AM437x, AMD Instinct GPUs gfx90x series. | | | |
| **Select publications** | | | |
| * Accelerated Erasure Coding: https://www.snia.org/events/storage-developer/presentations18. * <https://www.networkcomputing.com/storage/how-erasure-coding-evolving/155400422> * <http://www.tldp.org/LDP/LG/issue93/bhaskaran.html> | | | |